32x32 Video Crosspoint

The ISL59532 is a 300MHz 32x32 Video Crosspoint Switch. Each input has an integrated DC-restore clamp and an input buffer. Each output has a fast On-Screen Display (OSD) switch (for inserting graphics or other video) and an output buffer. The switch is non-blocking, so any combination of inputs to outputs can be chosen, including one channel driving multiple outputs. The Broadcast Mode directs one input to all 32 outputs. The output buffers can be individually controlled through the SPI interface, the gain can be programmed to x1 or x2, and each output can be placed into a high impedance mode.

The ISL59532 offers a typical -3dB signal bandwidth of 300MHz. Differential gain of 0.025% and differential phase of 0.05°, along with 0.1dB flatness out to 50MHz, make the ISL59532 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible three-wire serial interface. The ISL59532 interface is designed to facilitate both fast updates and initialization. On power-up, all outputs are high impedance to avoid output conflicts.

The ISL59532 is available in a 356 ball BGA package and specified over an extended -40°C to +85°C temperature range.

The single-supply ISL59532 can accommodate input signals from 0V to 3.5V and output voltages from 0V to 3.8V. Each input includes a clamp circuit that restores the input level to an externally applied reference in AC-coupled applications.

The ISL59533 is a fully differential input version of this device.

Features

- 32x32 non-blocking switch with buffered inputs and outputs
- 300MHz typical bandwidth
- 0.025%/0.05° dG/dP
- Output gain switchable x1 or x2 for each channel
- Individual outputs can be put in a high impedance state
- -90dB Isolation at 6MHz
- SPI digital interface
- Single +5V supply operation
- Pb-free (RoHS compliant)

Applications

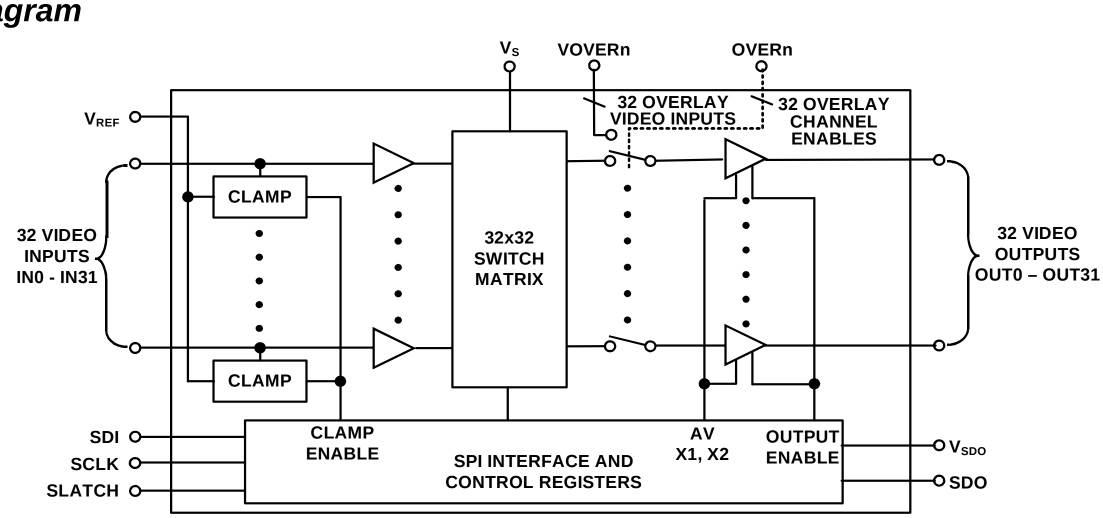
- Security camera switching
- RGB routing
- HDTV routing

Ordering Information

PART NUMBER	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59532IKEZ	-	356 Ld BGA	V356.27x27A

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pinout

ISL59532
(356 LD BGA)
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	In24	In25	In26	In27	In28	In29	In30	In31		Over31	Over30	Over29	Over28	Out27	Out26	Out25	Out24			
B										Out31	Out30	Out29	Out28	Over27	Over26	Over25	Over24			
C	In23									Vover31	Vover30	Vover29	Vover28	Vover27	Vover26	Vover25	Vover24	Vover23	Out23	Over23
D	In22		V_{SDO}	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vover22	Out22	Over22
E	In21			Vs	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	Vs	Vover21	Out21	Over21
F	In20			Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover20	Out20	Over20
G	In19		SDO	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover19	Over19	Out19
H	In18		RESET	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover18	Over18	Out18
J	In17		SLATCH	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover17	Over17	Out17
K	In16		SCLK	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover16	Over16	Out16
L	In15		SDI	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover15	Out15	Over15
M	In14		V_{REF}	Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover14	Out14	Over14
N	In13			Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover13	Out13	Over13
P	In12			Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover12	Out12	Over12
R	In11			Vs	⊕	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	⊕	Vs	Vover11	Over11	Out11
T	In10			Vs	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	Vs	Vover10	Over10	Out10
U	In9			Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vover9	Over9	Out9
V	In8				NC	NC			NC	Vover0	Vover1	Vover2	Vover3	Vover4	Vover5	Vover6	Vover7	Vover8	Over8	Out8
W										Over0	Over1	Over2	Over3	Out4	Out5	Out6	Out7			
Y	In7	In6	In5	In4	In3	In2	In1	In0		Out0	Out1	Out2	Out3	Over4	Over5	Over6	Over7			

⊕ = NO BALLS

BALLS LABELLED "NC" SHOULD BE LEFT UNCONNECTED - DO NOT TIE THEM TO GROUND!
BALLS WITH NO LABELS MAY BE TIED TO GROUND TO SLIGHTLY REDUCE THERMAL IMPEDANCE.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S and GND 6.0V
Maximum Continuous Output Current 40mA
Maximum power supply (V_S) slew rate 1V/µs

Operating Conditions

ESD Classification
Human Body Model 1500V
Machine Model 100V
Ambient Operating Temperature . . . . -40°C to +85°C

Thermal Information

Maximum Die Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

DC Electrical Specifications

V_S = 5V, R_L = 150Ω unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
V_S	Power Supply Voltage		4.5		5.5	V
V_{SDO}	Power Supply for SDO output pin	Establishes serial data output high level	1.2		5.5	V
A_V	Gain	A_V = 1	0.98	1	1.02	V/V
		A_V = 2	1.96	2	2.04	V/V
GM	Gain Matching (to average of all other outputs)	A_V = 1	-1.5		+1.5	%
		A_V = 2	-1.5		+1.5	%
V_{IN}	Video Input Voltage Range	A_V = 1	0		3.5	V
V_{OUT}	Video Output Voltage Range	A_V = 2	0.1		3.8	V
I_B	Input Bias Current	Clamp function disabled (DC coupled inputs)	-10	-5	1	µA
		Clamp function enabled, V_{IN} = V_{REF} + 0.5V	0.5	2	10	µA
I_{REF}	V_{REF} Input Current	Clamp function enabled		-110		µA
V_{OS}	Output Offset Voltage	A_V = 1	-20	8	35	mV
		A_V = 2	-100	-24	40	mV
I_{OUT}	Output Current	Sourcing, R_L = 10Ω to GND	60	108		mA
		Sinking, R_L = 10Ω to 2.5V	24	31		mA
PSRR	Power Supply Rejection Ratio	A_V = 2	50	70		dB
I_S	Supply Current	Enabled, all outputs enabled, no load current	560	640	720	mA
		Enabled, all outputs disabled, no load current	280	320	360	mA
		Disabled	1.2	1.8	2.4	mA

AC Electrical Specifications

V_S = 5V, R_L = 150Ω unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
BW -3dB	3dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		300		MHz
BW 0.1dB	0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		50		MHz
SR	Slew Rate	V_{OUT} = 2V_{P-P}, A_V = 2	300	520	740	V/µs
T_S	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}, A_V = 2		12		ns
Glitch	Switching Glitch, Peak	A_V = 1		40		mV
T_{over}	Overlay Delay Time	From OVER rising edge to output transition		6		ns
dG	Diff Gain	A_V = 2, R_L = 150Ω		0.025		%
dP	Diff Phase	A_V = 2, R_L = 150Ω		0.05		°
$XT_{ADJACENT}$	Adjacent Channel Crosstalk	6MHz, A_V = 1		-90		dB
$XT_{HOSTILE}$	Hostile Crosstalk	6MHz, A_V = 1		-72		dB
V_N	Input Referred Noise Voltage			18		nV/√Hz

NOTE:

1. All Min/Max parameters are guaranteed by 100% production testing at T_A = +25°C. Typical values are for information purposes only.

Pin Descriptions

NAME	NUMBER	DESCRIPTION
IN0	Y8	Crosspoint Video Input
IN1	Y7	Crosspoint Video Input
IN2	Y6	Crosspoint Video Input
IN3	Y5	Crosspoint Video Input
IN4	Y4	Crosspoint Video Input
IN5	Y3	Crosspoint Video Input
IN6	Y2	Crosspoint Video Input
IN7	Y1	Crosspoint Video Input
IN8	V1	Crosspoint Video Input
IN9	U1	Crosspoint Video Input
IN10	T1	Crosspoint Video Input
IN11	R1	Crosspoint Video Input
IN12	P1	Crosspoint Video Input
IN13	N1	Crosspoint Video Input
IN14	M1	Crosspoint Video Input
IN15	L1	Crosspoint Video Input
IN16	K1	Crosspoint Video Input
IN17	J1	Crosspoint Video Input
IN18	H1	Crosspoint Video Input
IN19	G1	Crosspoint Video Input
IN20	F1	Crosspoint Video Input
IN21	E1	Crosspoint Video Input
IN22	D1	Crosspoint Video Input
IN23	C1	Crosspoint Video Input
IN24	A1	Crosspoint Video Input
IN25	A2	Crosspoint Video Input
IN26	A3	Crosspoint Video Input
IN27	A4	Crosspoint Video Input
IN28	A5	Crosspoint Video Input
IN29	A6	Crosspoint Video Input
IN30	A7	Crosspoint Video Input
IN31	A8	Crosspoint Video Input
OUT0	Y10	Crosspoint Video Output
OUT1	Y11	Crosspoint Video Output
OUT2	Y12	Crosspoint Video Output
OUT3	Y13	Crosspoint Video Output
OUT4	W14	Crosspoint Video Output
OUT5	W15	Crosspoint Video Output

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
OUT6	W16	Crosspoint Video Output
OUT7	W17	Crosspoint Video Output
OUT8	V20	Crosspoint Video Output
OUT9	U20	Crosspoint Video Output
OUT10	T20	Crosspoint Video Output
OUT11	R20	Crosspoint Video Output
OUT12	P19	Crosspoint Video Output
OUT13	N19	Crosspoint Video Output
OUT14	M19	Crosspoint Video Output
OUT15	L19	Crosspoint Video Output
OUT16	K20	Crosspoint Video Output
OUT17	J20	Crosspoint Video Output
OUT18	H20	Crosspoint Video Output
OUT19	G20	Crosspoint Video Output
OUT20	F19	Crosspoint Video Output
OUT21	E19	Crosspoint Video Output
OUT22	D19	Crosspoint Video Output
OUT23	C19	Crosspoint Video Output
OUT24	A17	Crosspoint Video Output
OUT25	A16	Crosspoint Video Output
OUT26	A15	Crosspoint Video Output
OUT27	A14	Crosspoint Video Output
OUT28	B13	Crosspoint Video Output
OUT29	B12	Crosspoint Video Output
OUT30	B11	Crosspoint Video Output
OUT31	B10	Crosspoint Video Output
OVER0	W10	Overlay Logic Control (with pull-down)
OVER1	W11	Overlay Logic Control (with pull-down)
OVER2	W12	Overlay Logic Control (with pull-down)
OVER3	W13	Overlay Logic Control (with pull-down)
OVER4	Y14	Overlay Logic Control (with pull-down)
OVER5	Y15	Overlay Logic Control (with pull-down)
OVER6	Y16	Overlay Logic Control (with pull-down)
OVER7	Y17	Overlay Logic Control (with pull-down)
OVER8	V19	Overlay Logic Control (with pull-down)
OVER9	U19	Overlay Logic Control (with pull-down)
OVER10	T19	Overlay Logic Control (with pull-down)
OVER11	R19	Overlay Logic Control (with pull-down)

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
OVER12	P20	Overlay Logic Control (with pull-down)
OVER13	N20	Overlay Logic Control (with pull-down)
OVER14	M20	Overlay Logic Control (with pull-down)
OVER15	L20	Overlay Logic Control (with pull-down)
OVER16	K19	Overlay Logic Control (with pull-down)
OVER17	J19	Overlay Logic Control (with pull-down)
OVER18	H19	Overlay Logic Control (with pull-down)
OVER19	G19	Overlay Logic Control (with pull-down)
OVER20	F20	Overlay Logic Control (with pull-down)
OVER21	E20	Overlay Logic Control (with pull-down)
OVER22	D20	Overlay Logic Control (with pull-down)
OVER23	C20	Overlay Logic Control (with pull-down)
OVER24	B17	Overlay Logic Control (with pull-down)
OVER25	B16	Overlay Logic Control (with pull-down)
OVER26	B15	Overlay Logic Control (with pull-down)
OVER27	B14	Overlay Logic Control (with pull-down)
OVER28	A13	Overlay Logic Control (with pull-down)
OVER29	A12	Overlay Logic Control (with pull-down)
OVER30	A11	Overlay Logic Control (with pull-down)
OVER31	A10	Overlay Logic Control (with pull-down)
VOVER0	V10	Overlay Video Input
VOVER1	V11	Overlay Video Input
VOVER2	V12	Overlay Video Input
VOVER3	V13	Overlay Video Input
VOVER4	V14	Overlay Video Input
VOVER5	V15	Overlay Video Input
VOVER6	V16	Overlay Video Input
VOVER7	V17	Overlay Video Input
VOVER8	V18	Overlay Video Input
VOVER9	U18	Overlay Video Input
VOVER10	T18	Overlay Video Input
VOVER11	R18	Overlay Video Input
VOVER12	P18	Overlay Video Input
VOVER13	N18	Overlay Video Input
VOVER14	M18	Overlay Video Input
VOVER15	L18	Overlay Video Input
VOVER16	K18	Overlay Video Input
VOVER17	J18	Overlay Video Input

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
VOVER18	H18	Overlay Video Input
VOVER19	G18	Overlay Video Input
VOVER20	F18	Overlay Video Input
VOVER21	E18	Overlay Video Input
VOVER22	D18	Overlay Video Input
VOVER23	C18	Overlay Video Input
VOVER24	C17	Overlay Video Input
VOVER25	C16	Overlay Video Input
VOVER26	C15	Overlay Video Input
VOVER27	C14	Overlay Video Input
VOVER28	C13	Overlay Video Input
VOVER29	C12	Overlay Video Input
VOVER30	C11	Overlay Video Input
VOVER31	C10	Overlay Video Input
V_{REF}	M3	DC-restore clamp reference input. In an AC-coupled configuration (DC-Restore clamp enabled), the sync tip of composite video inputs will be restored to this level. Set to 0.3 to 0.7V for optimum performance. In an DC-coupled configuration (DC-Restore clamp disabled), this pin should be tied to ground. **Do not let the V_{REF} pin float!** A floating **V_{REF}** pin drifts high and, if the clamp function is enabled, will cause all of the outputs to simultaneously try to drive ~4V DC into their 150Ω loads.
SLATCH	J3	Serial Latch. Serial data is latched into ISL59532 on rising edge of SLATCH.
SCLK	K3	Serial data clock
SDI	L3	Serial data input
SDO	G3	Serial data output. Can be tied to SDI of another ISL59532 to enable daisy-chaining of multiple devices.
RESET	H3	Reset input. Pull high then low to reset device, but not needed in normal operation. Tie to ground in final application.
V_{SDO}	D3	Power supply for SDO pin. Tie to +5V for a 0 to 5V SDO output signal swing.
V_S		+5V power supply
GND		Ground
NC		No Connect - *Do not electrically connect to anything, including ground*.

Typical Performance Curves

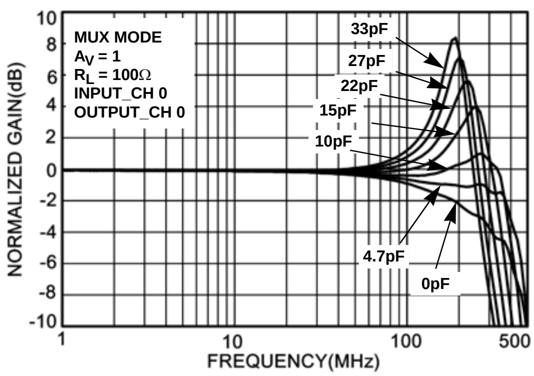


FIGURE 1. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, MUX MODE

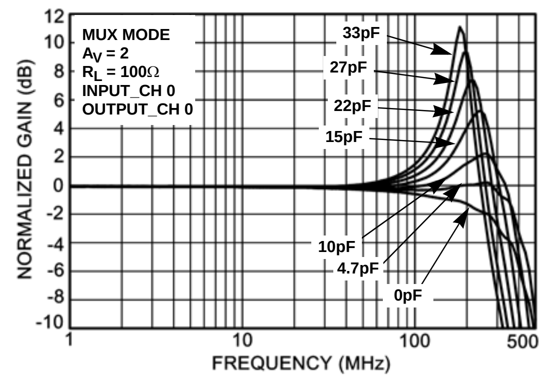


FIGURE 2. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, MUX MODE

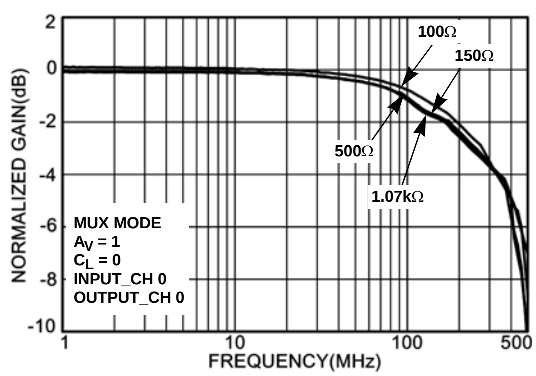


FIGURE 3. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, MUX MODE

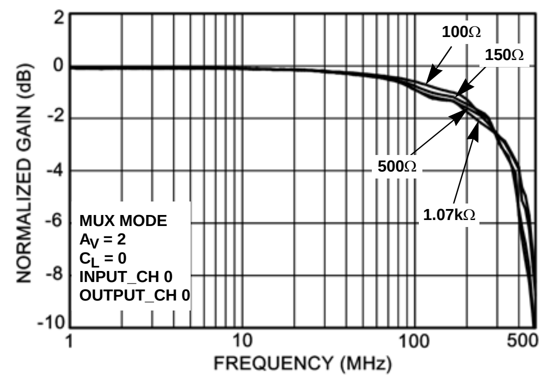


FIGURE 4. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, MUX MODE

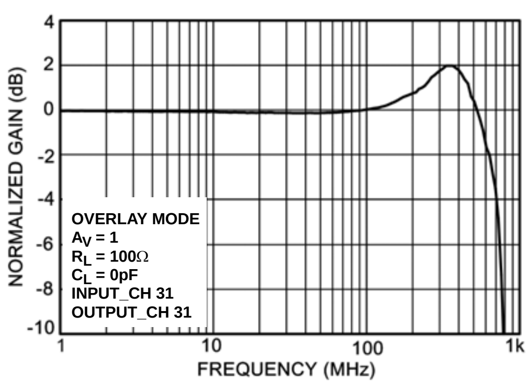


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 1

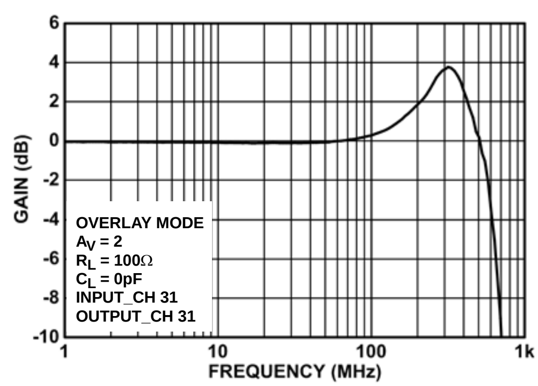


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 2

Typical Performance Curves (Continued)

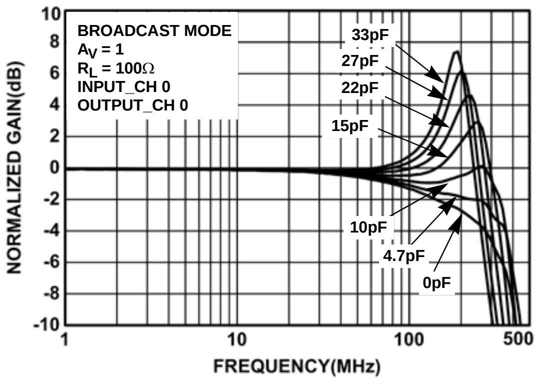


FIGURE 7. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, BROADCAST MODE

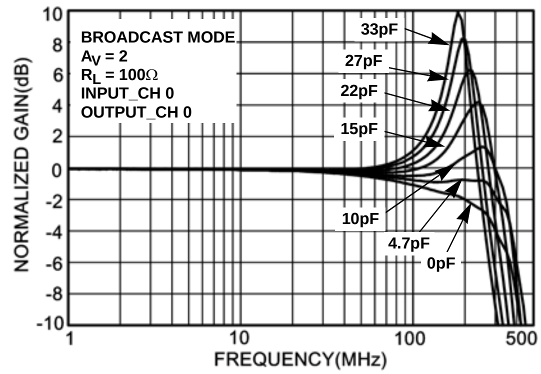


FIGURE 8. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, BROADCAST MODE

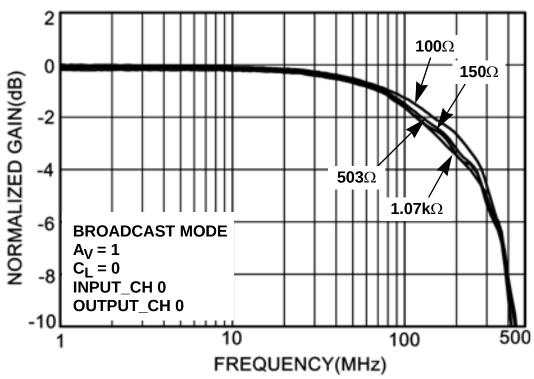


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, BROADCAST MODE

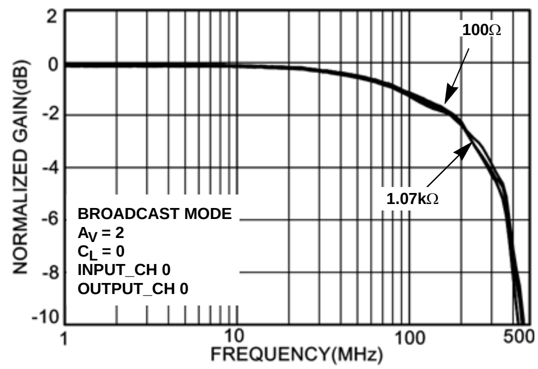


FIGURE 10. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, BROADCAST MODE

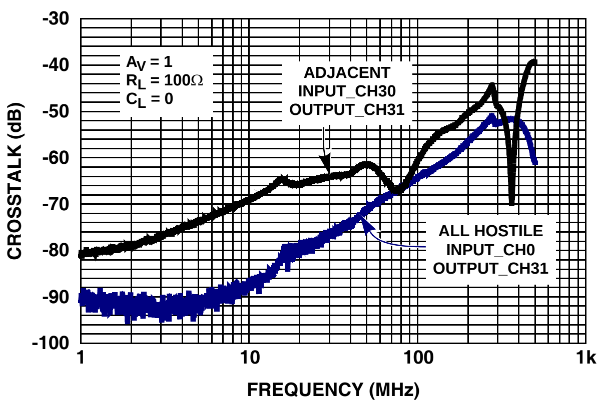


FIGURE 11. CROSSTALK - A_V = 1

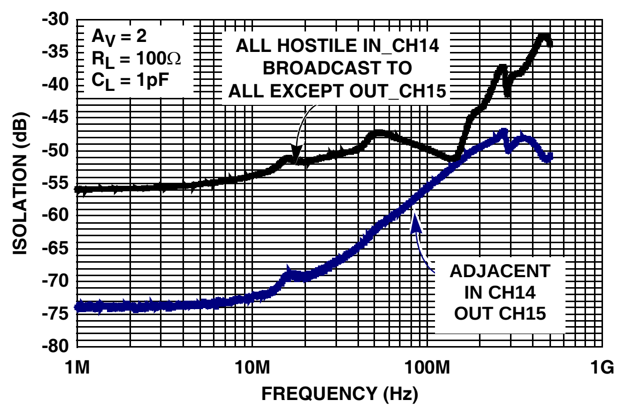


FIGURE 12. CROSSTALK - A_V = 2

Typical Performance Curves (Continued)

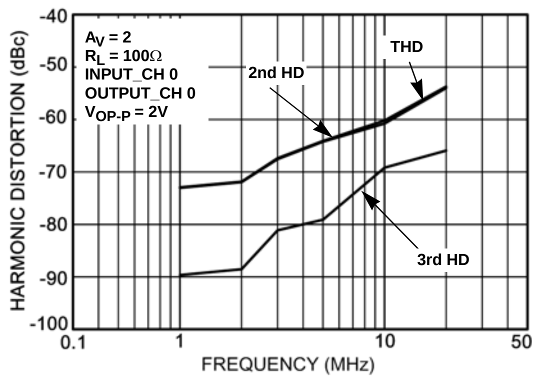


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

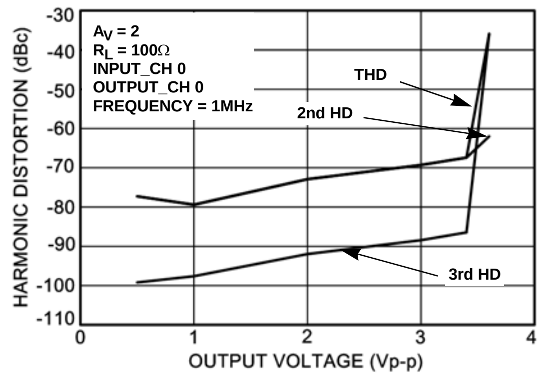


FIGURE 14. HARMONIC DISTORTION vs V_{OUT_P-P}

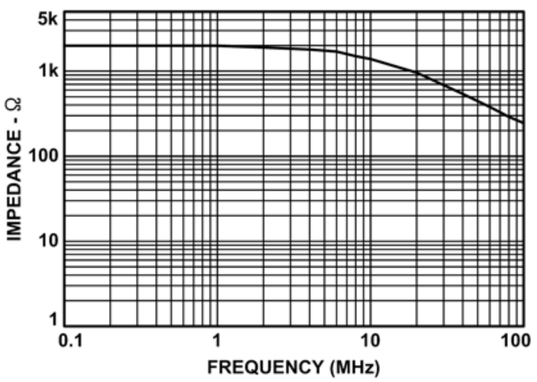


FIGURE 15. DISABLED OUTPUT IMPEDANCE

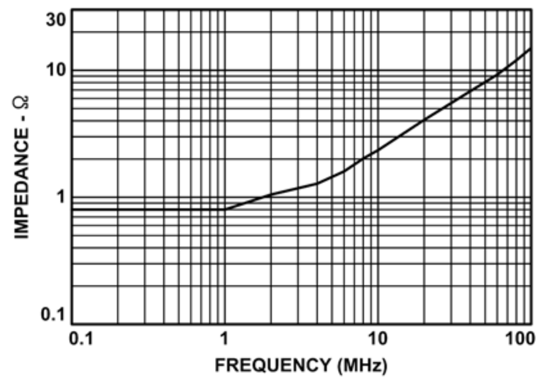


FIGURE 16. ENABLED OUTPUT IMPEDANCE

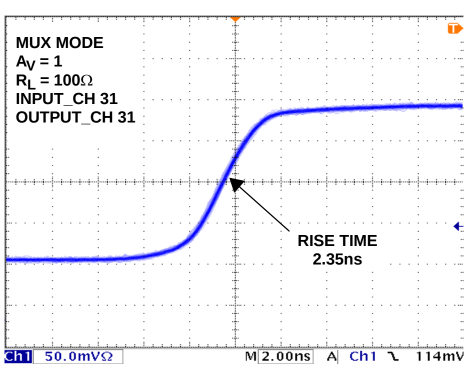


FIGURE 17. RISE TIME - $A_V = 1$

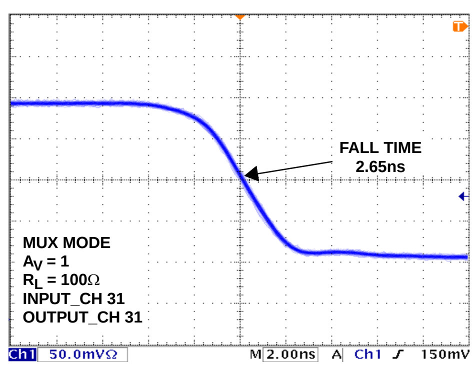


FIGURE 18. FALL TIME - $A_V = 1$

Typical Performance Curves (Continued)

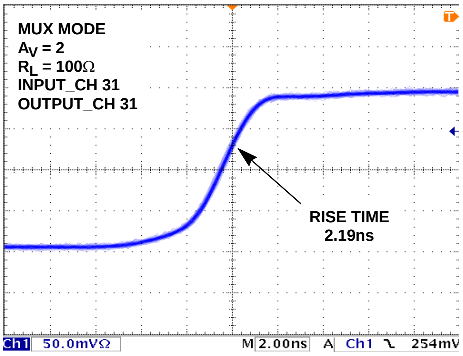


FIGURE 19. RISE TIME - $A_V = 2$

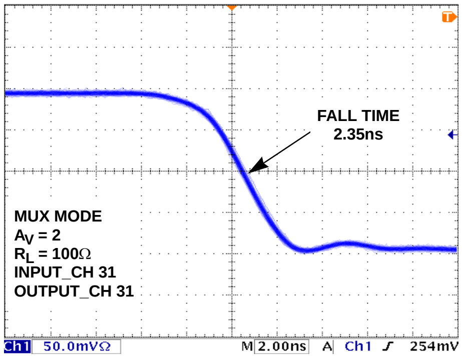


FIGURE 20. FALL TIME - $A_V = 2$

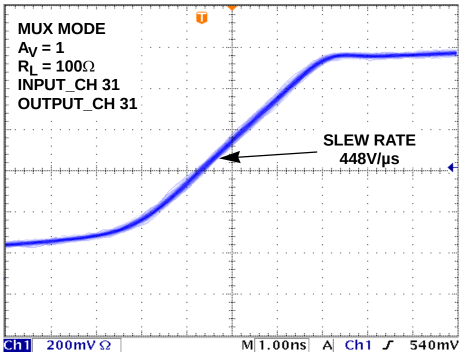


FIGURE 21. RISING SLEW RATE - $A_V = 1$

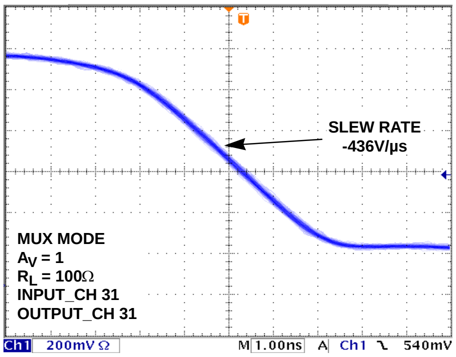


FIGURE 22. FALLING SLEW RATE - $A_V = 1$

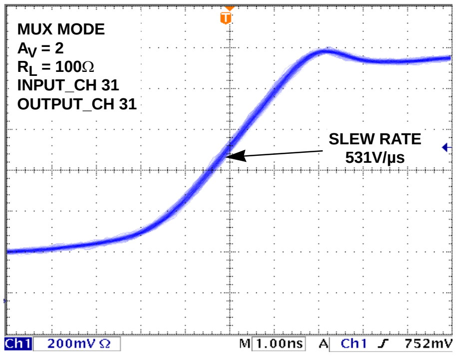


FIGURE 23. RISING SLEW RATE - $A_V = 2$

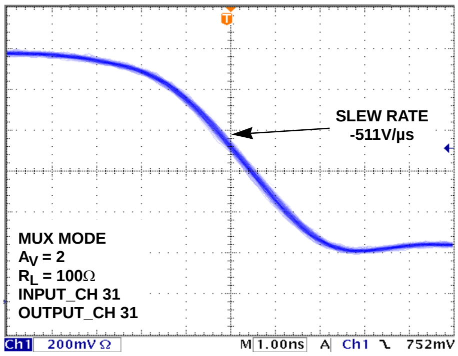


FIGURE 24. FALLING SLEW RATE - $A_V = 2$

Typical Performance Curves (Continued)

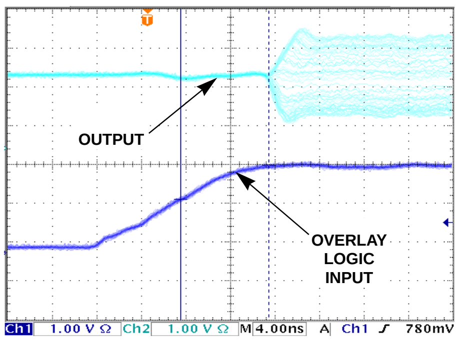


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

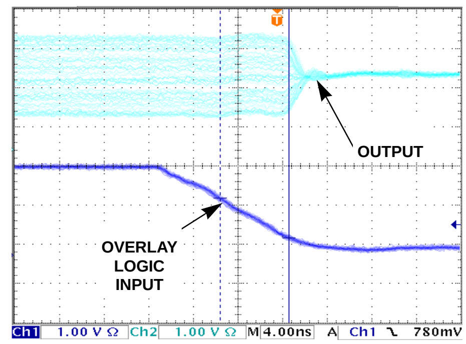


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

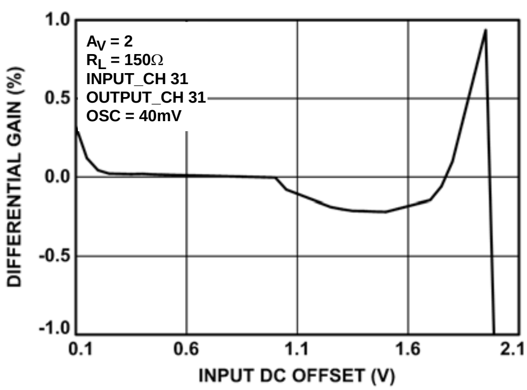


FIGURE 27. DIFFERENTIAL GAIN, A_V = 2

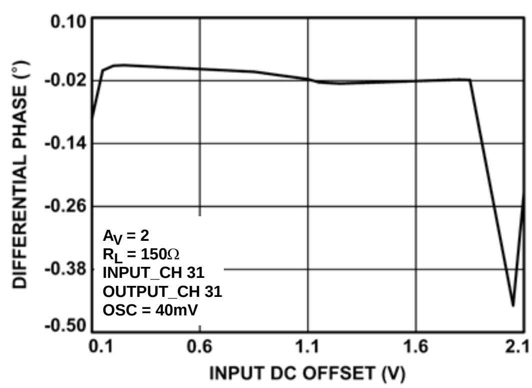


FIGURE 28. DIFFERENTIAL PHASE, A_V = 2

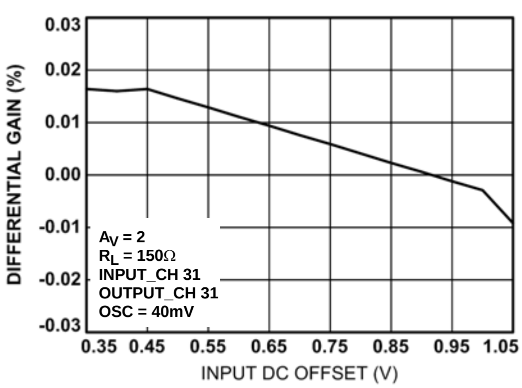


FIGURE 29. DIFFERENTIAL GAIN, A_V = 2

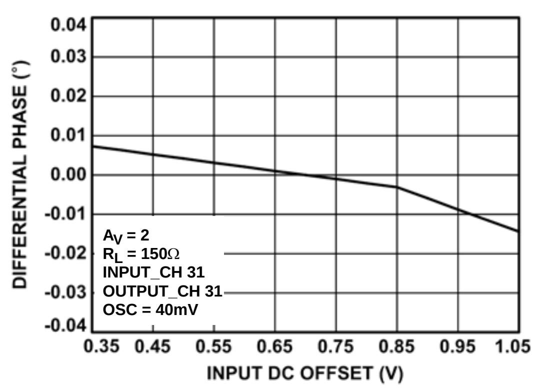


FIGURE 30. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curves (Continued)

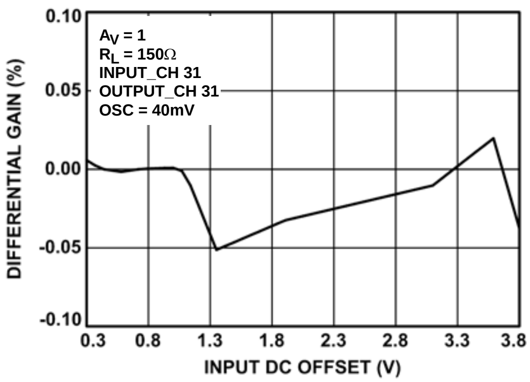


FIGURE 31. DIFFERENTIAL GAIN, $A_V = 1$

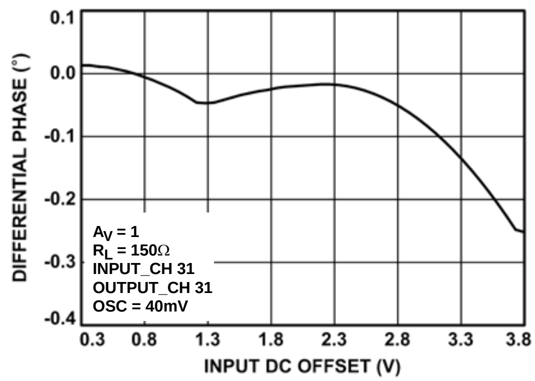


FIGURE 32. DIFFERENTIAL PHASE, $A_V = 1$

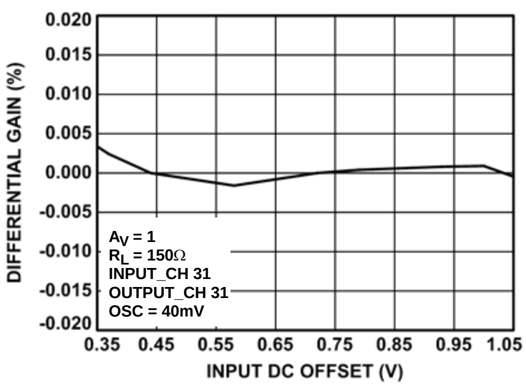


FIGURE 33. DIFFERENTIAL GAIN, $A_V = 1$

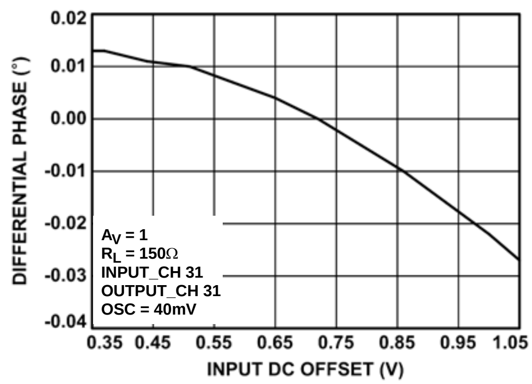


FIGURE 34. DIFFERENTIAL GAIN, $A_V = 1$

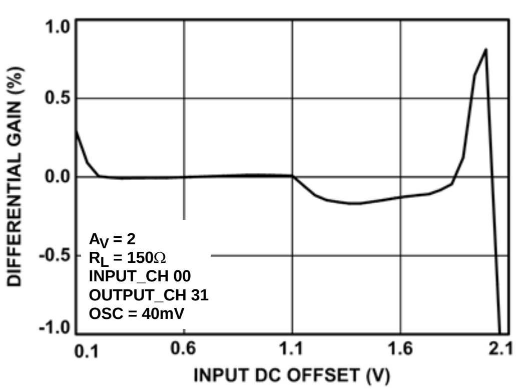


FIGURE 35. DIFFERENTIAL GAIN, $A_V = 2$

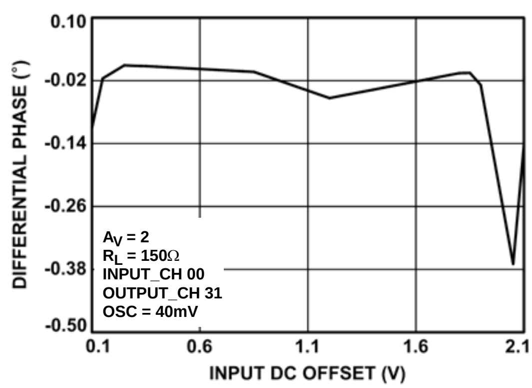


FIGURE 36. DIFFERENTIAL PHASE, $A_V = 2$

Typical Performance Curves (Continued)

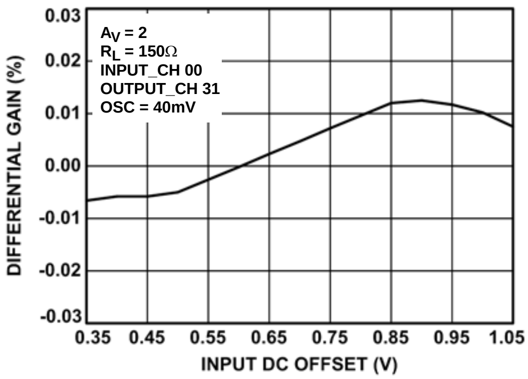


FIGURE 37. DIFFERENTIAL GAIN, A_V = 2

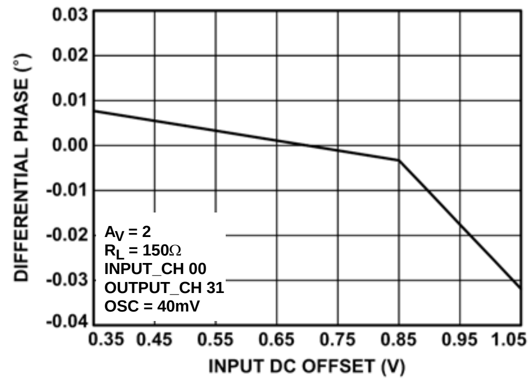


FIGURE 38. DIFFERENTIAL PHASE, A_V = 2

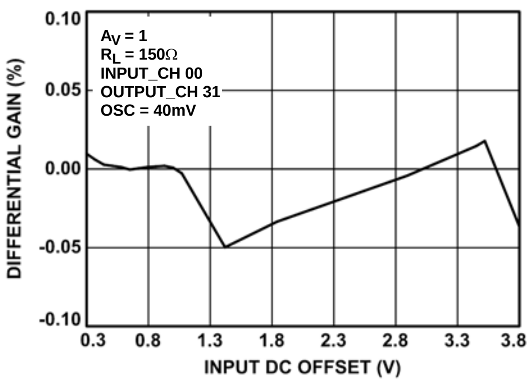


FIGURE 39. DIFFERENTIAL GAIN, A_V = 1

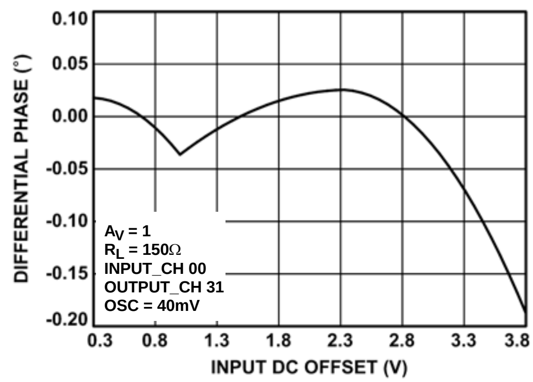


FIGURE 40. DIFFERENTIAL PHASE, A_V = 1

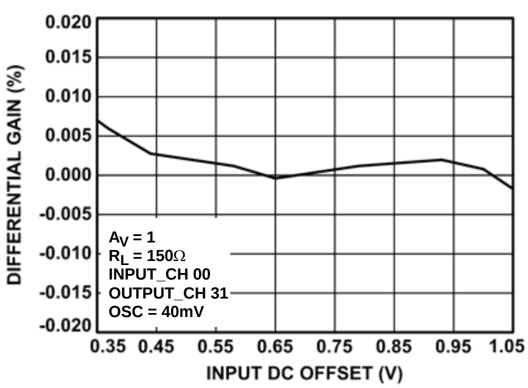


FIGURE 41. DIFFERENTIAL GAIN, A_V = 1

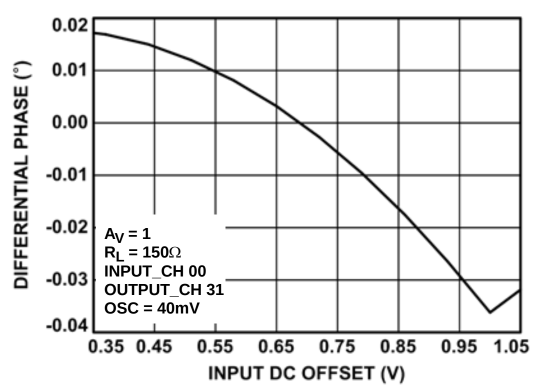


FIGURE 42. DIFFERENTIAL PHASE, A_V = 1

Typical Performance Curves (Continued)

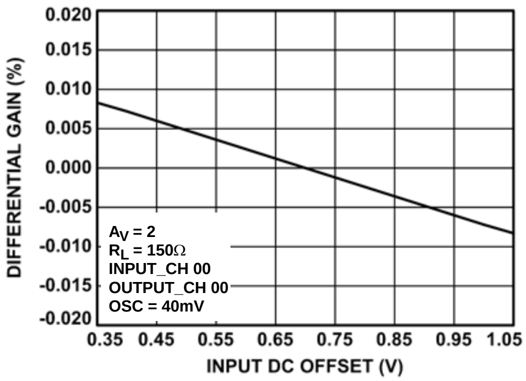


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY, A_V = 2

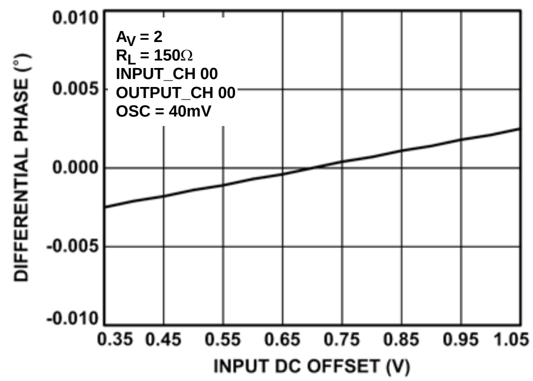


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY, A_V = 2

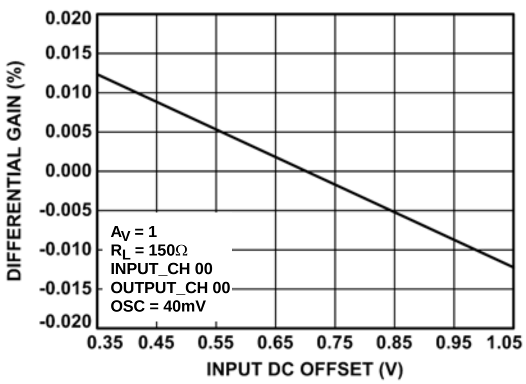


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY, A_V = 1

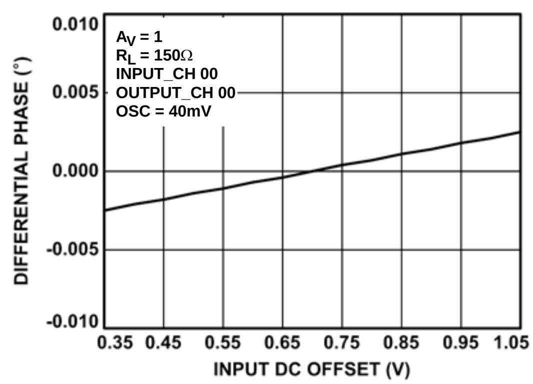


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY, A_V = 1

3dB Bandwidth, MUX Mode, $A_V = 1$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
OUTPUT CHANNELS	0	262					270					268					235					236					235						236
	1		224																													214	
	2			217																											214		
	3				211																									203			
	4					277																							272				
	5	267					268										247											268					259
	6							288																			290						
	7								271																	278							
	8									269															271								
	9										277													275									
	10	273										274					256						272										267
	11												274									272											
	12													255							258												
	13														264					271													
	14															268			274														
	15	298	292	289	290	304	299	307	304	198	309	299	300	292	290	286	283	290	292	299	296	298	308	326	311	221	309	313	311	293	297	294	283
	16																278	286															
	17															268			276														
	18														265					277													
	19													255							264												
	20	281											282				265					288											283
	21											266											275										
	22										285													350									
	23									268															336								
	24								196																	216							
	25	264						271									247										277						272
	26						269																					285					
	27					267																							283				
	28				199																									281			
	29			206																											252		
	30		214																													252	
	31	238					230					238					220					280					287						274

3dB Bandwidth, MUX Mode, $A_V = 2$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	304					323					324					305					313					320						308
	1		291																													290	
	2			290																											294		
	3				302																									295			
	4					353																							348				
	5	346					349										310											348					331
	6							371																			370						
	7								372																	376							
	8									360															366								
	9										363													363									
	10	351										350					317						350										340
	11												337									336											
	12													348							350												
	13														340					351													
	14															327			341														
	15	360	353	348	349	366	360	366	363	280	366	357	360	348	348	343	337	348	352	358	353	356	364	372	366	173	364	367	368	348	354	352	352
	16																325	338															
	17															330			345														
	18														339					355													
	19													344							350												
	20	351											350				321					354											348
	21											347											353										
	22										371													381									
	23									361															377								
	24								289																	334							
	25	354						360									300										360						353
	26						350																					366					
	27					338																							357				
	28				288																									348			
	29			290																											318		
	30		295																													308	
	31	311					313					314					297					336					345						314

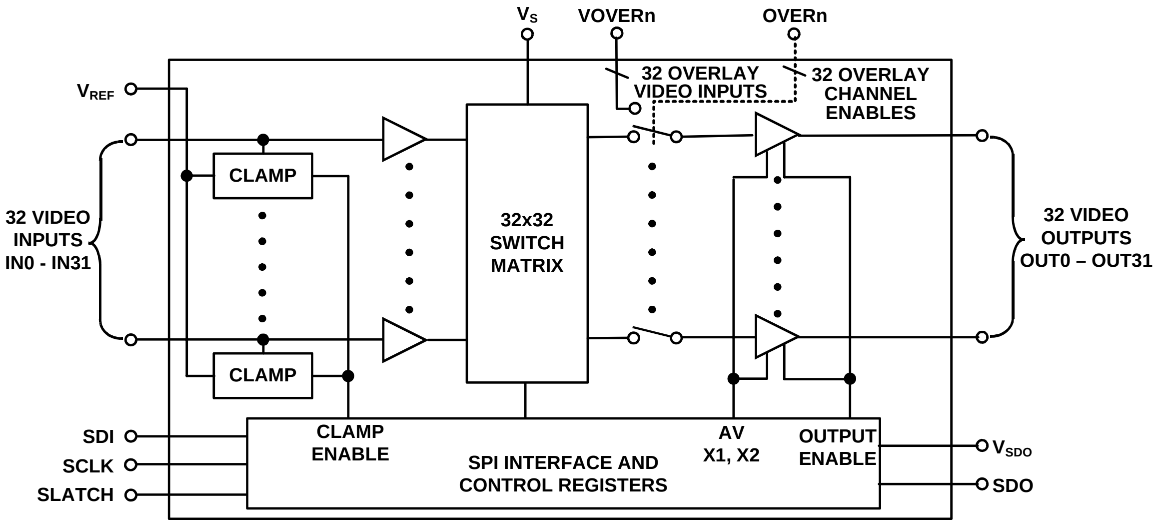
3dB Bandwidth, Broadcast Mode, $A_V = 1$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	196	204	193	175	154	154	158	161	169	157	155	146	125	121	115	109	81	81	79	80	85	85	86	86	83	82	82	77	80	82	85	86
	1	185	189														104															85	87
	2	172		163													104														85		87
	3	161			138												99													81			87
	4	165				128											99												79				89
	5	160					126										97											82					89
	6	152						123									95										81						89
	7	141							119								91									84							89
	8	133								113							86								82								89
	9	133									113						90							85									90
	10	132										113					91						88										92
	11	130											107				90					90											93
	12	125												94			87				81												92
	13	125													91		88			84													95
	14	127														90	88		85														97
	15	125	129	124	118	109	109	110	112	113	110	107	106	95	93	91	89	88	88	88	88	95	94	96	97	93	92	89	86	91	93	95	98
	16	124															89	88															100
	17	119														85	85		86														100
	18	116													88		84			87													100
	19	113												89			82				88												100
	20	114											97				84					98											102
	21	112										99					82						98										103
	22	108									94						80							100									102
	23	107								96							78								100								104
	24	106							96								79									99							106
	25	107						96									80										99						110
	26	108					96										81											98					114
	27	107				97											81												99				123
	28	104			98												78													105			115
	29	104		102													80														106		119
	30	105	106														80															118	125
	31	107	110	108	103	98	98	98	99	101	99	97	95	87	86	84	81	113	112	112	114	126	126	128	129	124	118	114	111	120	122	129	131

3dB Bandwidth, Broadcast Mode, $A_V = 2$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	270	277	268	247	213	216	227	244	258	223	208	196	147	142	132	123	85	85	85	86	91	91	92	93	90	88	86	85	89	90	92	94
	1	256	261														117															93	93
	2	240		223													112														88		92
	3	219			189												106													86			92
	4	233				158											108												83				95
	5	225					152										106											86					95
	6	204						146									105										88						95
	7	187							137								99									89							94
	8	172								128							92								85								94
	9	171									128						96							93									96
	10	170										126					97						94										98
	11	167											119				97					96											101
	12	152												103			93				89												99
	13	153													99		93			88													103
	14	155														96	94		89														105
	15	151	155	146	134	123	125	126	126	128	123	123	114	103	99	97	94	94	92	92	93	102	102	102	102	99	99	93	93	98	99	102	104
	16	146															93	94															109
	17	138														91	91		92														109
	18	133													94		90			93													109
	19	127												95			90				94												109
	20	129											106				89					106											113
	21	126										106					86						105										114
	22	119									102						84							107									112
	23	118								105							83								106								114
	24	116							103								83									107							117
	25	118						103									84										107						125
	26	120					103										84											108					135
	27	118				103											85												108				142
	28	113			106												82													113			133
	29	114		110													81														123		143
	30	115	116														82															138	155
	31	117	121	118	112	105	105	106	108	110	107	104	101	93	91	88	85	130	127	127	130	153	150	158	163	149	140	133	126	140	146	161	164

Block Diagram



General Description

The ISL59532 is a 32x32 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be generated from any of the 32 input video signal sources, and each output can have OSD information inserted through a dedicated, fast 2:1 mux located before the output buffer. There is also a Broadcast mode allowing any one input to be broadcast to all 32 outputs. A DC restore clamp function enables the ISL59532 to AC-couple incoming video.

The ISL59532 offers a -3dB signal bandwidth of 300MHz. Differential gain and differential phase of 0.025% and 0.05° respectively, along with 0.1dB flatness out to 50MHz make this ideal for multiplexing composite NTSC and PAL signals. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59532 interface is designed to facilitate both fast initialization and configuration changes. On power-up, all outputs are initialized to the disabled state to avoid output conflicts in the user’s system.

Digital Interface

The ISL59532 uses a serial interface to program the configuration registers. The serial interface uses three signals (SCLK, SDI, and SLATCH) for programming the ISL59532, while a fourth signal (SDO) enables optional daisy-chaining of multiple devices. The serial clock can run at up to 5MHz (5Mbits/s).

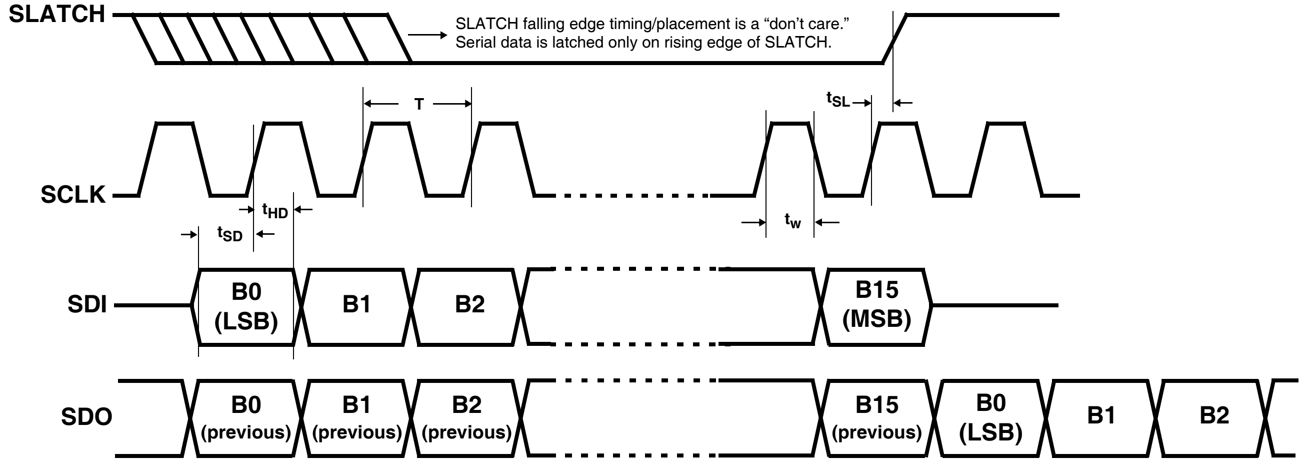
Serial Interface

The ISL59532 is programmed through a simple serial interface. Data on the SDI (serial data input) pin is shifted into a 16-bit shift register on the rising edge of the SCLK (serial clock) signal. (This is continuously done regardless of the state of the SLATCH signal.) The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see the Serial Timing Diagram). After all 16 bits of data have been loaded into the shift register, the rising edge of SLATCH updates the internal registers.

While the ISL59532 has an SDO (Serial Data Out) pin, it does not have a register readback feature. The data on the SDO pin is an exact replica of the incoming data on the SDI pin, delayed by 15.5 SCLKs (an input bit is latched on the rising edge of SLCK, and is output on SDO on the falling edge of SLCK 15.5 SCLKs later). Multiple ISL59532’s can be daisy-chained by connecting the SDO of one to the SDI of the other, with SCLK and SLATCH common to all the daisy-chained parts. After all the serial data is transmitted (16 bits * n devices = 16*n SCLKs), the rising edge of SLATCH will update the configuration registers of all n devices simultaneously.

The Serial Timing Diagram and Serial Timing Parameters table on page 19 show the timing requirements for the serial interface.

Serial Timing Diagram



SDO = SDI delayed by 15.5 SCLKs to allow daisy-chaining of multiple ISL59532s. SDO changes on the falling edge of SCLK.

TABLE 1. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	SCLK period
t_W	0.50 * T	Clock Pulse Width
t_{SD}	≥20ns	Data Setup Time
t_{HD}	≥20ns	Data Hold Time
t_{SL}	≥20ns	Final SLCK rising edge (latching B15) to SLATCH rising edge

Programming Model

The ISL59532 is configured by a series of 16-bit serial control words. The three MSBs (B15-13) of each serial word determine the basic command:

TABLE 2. COMMAND FORMAT

B15	B14	B13	COMMAND	NUMBER OF WRITES
0	0	0	INPUT/OUTPUT: Maps input channels to output channels	32 (1 channel per write)
0	0	1	OUTPUT ENABLE: Output enable for individual channels	4 (8 channels per write)
0	1	0	GAIN SET: Gain (x1 or x2) for each channel	4 (8 channels per write)
0	1	1	BROADCAST: Enables broadcast mode and selects the input channel to be broadcast to all output channels	1
1	1	1	CONTROL: Clamp on/off, operational/standby mode, and global output enable/disable	1

Mapping Inputs to Outputs

Inputs are mapped to their desired outputs using the input/output control word. Its format is:

TABLE 3. INPUT/OUTPUT WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I_4	I_3	I_2	I_1	I_0	-	-	-	O_4	O_3	O_2	O_1	O_0

I_4:I_0 form the 5 bit word indicating the input channel (0 to 31), and O_4:O_0 determine the output channel which that input channel will map to. One input can be mapped to one or multiple outputs. To fully program the ISL59532, 32 INPUT/OUTPUT words must be transmitted - one for each input channel.

Note: Broadcast Mode must be disabled when configuring input/output mapping. INPUT/OUTPUT words transmitted while in Broadcast Mode will not be processed correctly and result in corrupt channel mapping when Broadcast Mode is disabled.

Enabling Outputs

The output enable control word is used to enable individual outputs. There are 32 channels to configure, so this is accomplished by writing 4 serial words, each controlling a bank of eight outputs at a time. The bank is selected by bits B9 and B8. The output enable control word format is:

TABLE 4. OUTPUT ENABLE FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	0	0	**0**	**0**	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	1	0	0	0	**0**	**1**	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8
0	0	1	0	0	0	**1**	**0**	O_{23}	O_{22}	O_{21}	O_{20}	O_{19}	O_{18}	O_{17}	O_{16}
0	0	1	0	0	0	**1**	**1**	O_{31}	O_{30}	O_{29}	O_{28}	O_{27}	O_{26}	O_{25}	O_{24}

Setting the O_N bit = 0 tri-states the output. Setting the O_N bit = 1 enables the output if the Global Output Enable bit is also set (the individual output enable bits are ANDed with the Global Output Enable bit before they are sent to the output stage).

Setting the Gain

The gain of each output may be set to x1 or x2 using the Gain Set word. It is in the same format as the output enable control word:

TABLE 5. GAIN SET FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	**0**	**0**	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0
0	1	0	0	0	0	**0**	**1**	G_{15}	G_{14}	G_{13}	G_{12}	G_{11}	G_{10}	G_9	G_8
0	1	0	0	0	0	**1**	**0**	G_{23}	G_{22}	G_{21}	G_{20}	G_{19}	G_{18}	G_{17}	G_{16}
0	1	0	0	0	0	**1**	**1**	G_{31}	G_{30}	G_{29}	G_{28}	G_{27}	G_{26}	G_{25}	G_{24}

Set G_N = 0 for a gain of x1 or 1 for a gain of x2.

Broadcast Mode

The Broadcast Mode routes one input to all 32 outputs. The broadcast control word is:

TABLE 6. BROADCAST FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I_4	I_3	I_2	I_1	I_0	0	0	0	0	0	0	0	Enable Broadcast 0: Broadcast Mode Disabled 1: Broadcast Mode Enabled

I_4:I_0 form the 5-bit word indicating the input channel (0 to 31) to be sent to all 32 outputs. Set the Enable Broadcast bit (B0) = 1 to enable Broadcast Mode, or to 0 to disable Broadcast Mode. When Broadcast Mode is disabled, the previous channel assignments are restored.

Control Word

The ISL59532's power-on reset disables all outputs and places the part in a low-power standby mode. To enable the device, the following control word should be sent:

TABLE 7. CONTROL WORD FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	0	0	Clamp 0: Clamp Disabled 1: Clamp Enabled	0	0	0	0	0	0	0	Power 0: Standby 1: Operational	Global Output Enable 0: All outputs tristated 1: Individual Output Enable bits control outputs

The Clamp bit enables the input clamp function, forcing the AC-coupled signal's most negative point to be equal to V_{REF}.

Note: The Clamp bit turns the DC-Restore clamp function on or off for *all* channels - there is no DC-Restore on/off control for individual channels. The DC-Restore function only works with signals with sync tips (composite video). Signals that do not have sync tips (the Chroma/C signal in s-video and the Pb, Pr signals in Component video), will be severely distorted if run through a DC-Restore/clamp function.

For this reason, the ISL59532 must be in DC-coupled mode (Clamp Disabled) to be compatible with s-video and component video signals.

Bandwidth Considerations

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, and the routing (the path from the input to the output), bandwidth can vary between 100MHz and 350MHz. A short discussion of the trade-offs — including matrix configuration, output buffer gain selection, channel selection, and loading — follows.

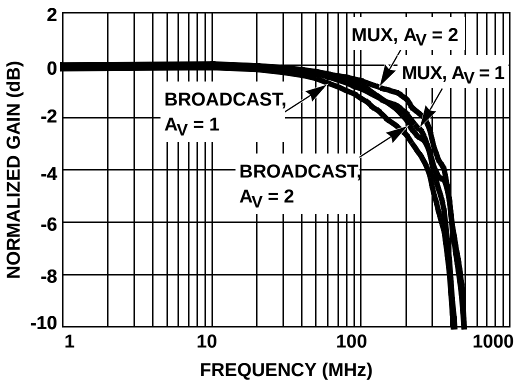


FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES

In multiplexer mode, one input typically drives one output channel, while in broadcast mode, one input drives all 32 outputs. As the number of outputs driven increases, the parasitic loading on that input increases. Broadcast Mode is the worst-case, where the capacitance of all 32 channels loads one input, reducing the overall bandwidth. In addition, due to internal device compensation, an output buffer gain of x2 has higher bandwidth than a gain of x1. Therefore, the highest bandwidth configuration is multiplexer mode (with each input mapped to only one output) and an output buffer gain of x2.

The relative locations of the input and output channels also have significant impact on the device bandwidth (due to the layout of the ISL59530 silicon). When the input and output channels are further away, there are additional parasitics as a result of the additional routing, resulting in lower bandwidth.

The bandwidth does not change significantly with resistive loading as shown in the typical performance curves. However several of the curves demonstrate that frequency response is sensitive to capacitance loading. This is most significant when laying out the PCB. If the PCB trace length between the output of the crosspoint switch and the back-termination resistor is not minimized, the additional parasitic capacitance will result in some peaking and eventually a reduction in overall bandwidth.

Linear Operating Region

In addition to bandwidth optimization, to get the best linearity the ISL59532 should be configured to operate in its most linear operating region. Figure 48 shows the differential gain curve. The ISL59532 is a single supply 5V design with its most linear region between 0.1 and 2V. This range is fine for most video signals whose nominal signal amplitude is 1V. The most negative input level (the sync tip for composite video) should be maintained at 0.3V or above for best operation.

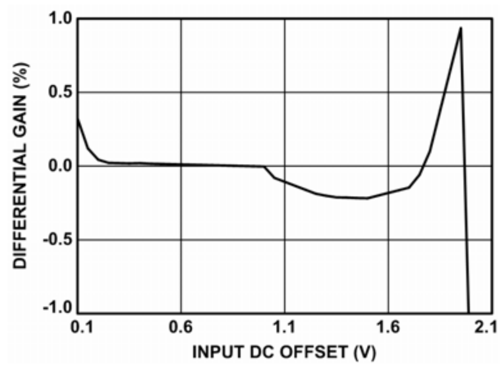


FIGURE 48. DIFFERENTIAL GAIN RESPONSE

In a DC-coupled application, it is the system designer's responsibility to ensure that the video signal is always in the optimum range.

When AC coupling, the ISL59532's Clamp (also called "DC restore") function automatically and continuously adjusts the DC level so that the most negative portion of the video is always equal to V_{REF}.

A discussion of the benefits of the DC restoration function begins by understanding the Clamp circuit shown in Figure 49. The incoming video signal is typically terminated into 75Ω, then AC coupled through C_1, at which point it is connected to the base of the buffer's diff pair. These components form the video path.

The Clamp function consists of Q_1, D_1, Q_2, D_2, the two current sources, and the 3 switches controlled by the Clamp Enable signal. The V_{REF} voltage is level-shifted up two diode drops (Q_1 and D_1) to the base of Q_2. If the voltage at the cathode of D_2 goes below V_{REF}, Q_2 and D_2 will turn on, keeping the IN_X voltage at V_{REF}. If the voltage at IN_X is greater than V_{REF}, Q_2 and D_2 are off and the IN_X node is high impedance. This is how the clamp function forces the lowest portion of the video signal (the sync tip) to always be equal to or greater than V_{REF}.

To make sure that the sync tip is always *equal to* (not equal to or greater than) V_{REF}, i_1 is constantly sinking ~2µA of current from C_1. This causes each sync tip to be slightly lower voltage than the previous sync tip, causing Q_2 and D_2 to turn on at each sync tip and raise the voltage to V_{REF}. The 2µA pulldown with a 0.1uF capacitor and a 15kHz HSYNC frequency results in 1.3mV of "droop" across every line, or

0.2% of the video signal. Because 1.3mV is only 0.2% of a 0.7V video signal, this droop is imperceptible to the human eye.

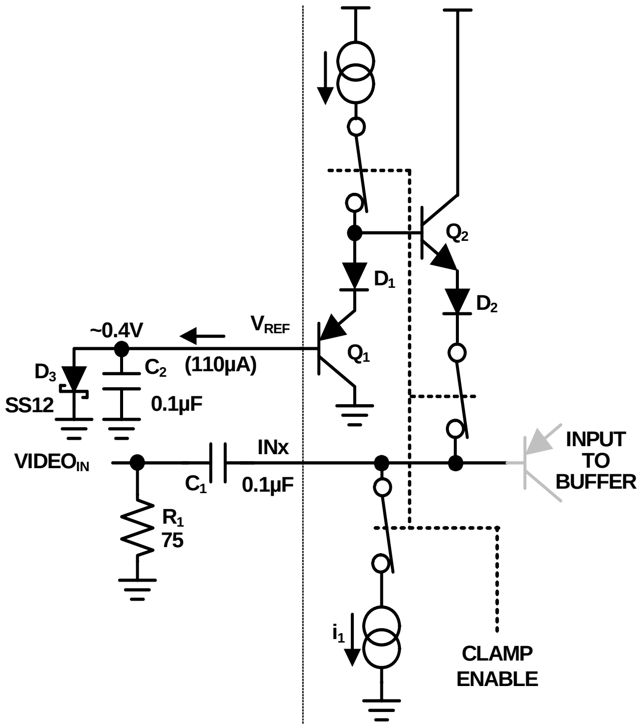


FIGURE 49. DC RESTORE BLOCK DIAGRAM

This is how the video is “DC-restored” after being AC coupled into the ISL59532. The sync tip voltage will be equal to V_{REF} on the right side of C_1, regardless of the DC level of the video on the left side of C_1. Due to various sources of offset in the actual clamp function, the actual sync tip level is typically about 75mV higher than V_{REF} (for V_{REF} = 0.4V).

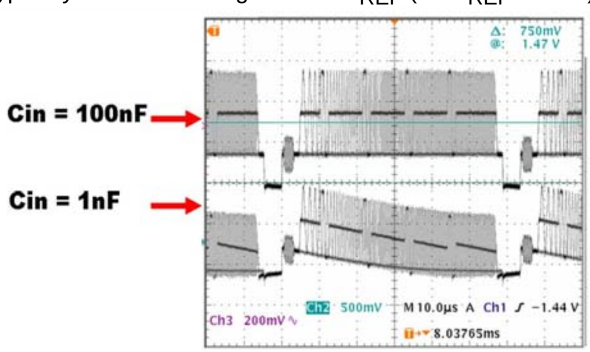


FIGURE 50. DC RESTORE VIDEO WAVEFORMS

It is important to choose the correct value for C_{IN}. Too small a value will generate too much droop, and the image will be visibly darker on the right than on the left. A C_{IN} value that is too large may cause the clamp to fail to converge. The droop rate (dV/dt) is i_1/C_{IN} volts/second. In general, the droop voltage should be limited to <1 IRE over a period of one line of video; so for 1 IRE = 7mV, I_B = 10µA maximum, and an NTSC waveform we will set C_{IN} > 10µA*60µs/7mV = 0.086µF. Figure 50 shows the result of C_{IN} = 0.1µF delivering acceptable droop and C_{IN} = 0.001µF producing excessive droop

When the clamp function is disabled in the CONTROL register (Clamp = 0) to allow DC-coupled operation, the I_{CLAMP} current sinks/sources are disabled and the input passes through the DC Restore block unaffected. In this application V_{REF} may be tied to GND.

Overlay Operation

The ISL59532 features an overlay feature, that allows an external video signal or DC level to be inserted in place of that output channel’s video. When the $OVER_N$ signal is taken high, the output signal on the OUT_N pin is replaced with the signal on the $VOVER_N$ pin.

There are several ways the overlay feature can be used. Toggling the $OVER_N$ signal at the frame rate or slower will replace the video frame(s) on the OUT_N pin with the video supplied on the $VOVER_N$ pin.

Another option (for OSD displays, for example), is to put a DC level on the $VOVER_N$ line and toggle the $OVER_N$ signal at the pixel rate to create a monocolor image “overlaid” on channel N’s output signal.

Finally, by enabling the $OVER_N$ signal for some portion of each line over a certain amount of lines, a picture-in-picture function can be constructed.

It’s important to note that the overlay inputs do not have the DC Restore function previously described - the overlay signal is DC coupled into the output. It is the system designer’s responsibility to ensure that the video levels are in the ISL59532’s linear region and matching the output channel’s offset and amplitude. One easy way to do this is to run the video to be overlaid through one of the ISL59532’s unused channels and then into the $VOVER_N$ input.

The $OVER_N$ pins all have weak pulldowns, so if they are unused, they can either be left unconnected or tied to GND.

Power Dissipation and Thermal Resistance

With a large number of switches, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

- T_{JMAX} = Maximum junction temperature = +125°C
- T_{AMAX} = Maximum ambient temperature = +85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} \quad \text{(EQ. 2)}$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 700mA
- V_{OUT} = Maximum output voltage of the application = 2V
- R_{LOAD} = Load resistance tied to ground = 150
- n = 1 to 32 channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 4.8W \quad \text{(EQ. 3)}$$

The required θ_{JA} to dissipate 4.8W is:

$$\Theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 8.33(°C/W) \quad \text{(EQ. 4)}$$

Table 8 shows θ_{JA} thermal resistance results with a Wakefield heatsink and without heatsink and various airflow. At the thermal resistance equation shows, the required thermal resistance depends on the maximum ambient temperature.

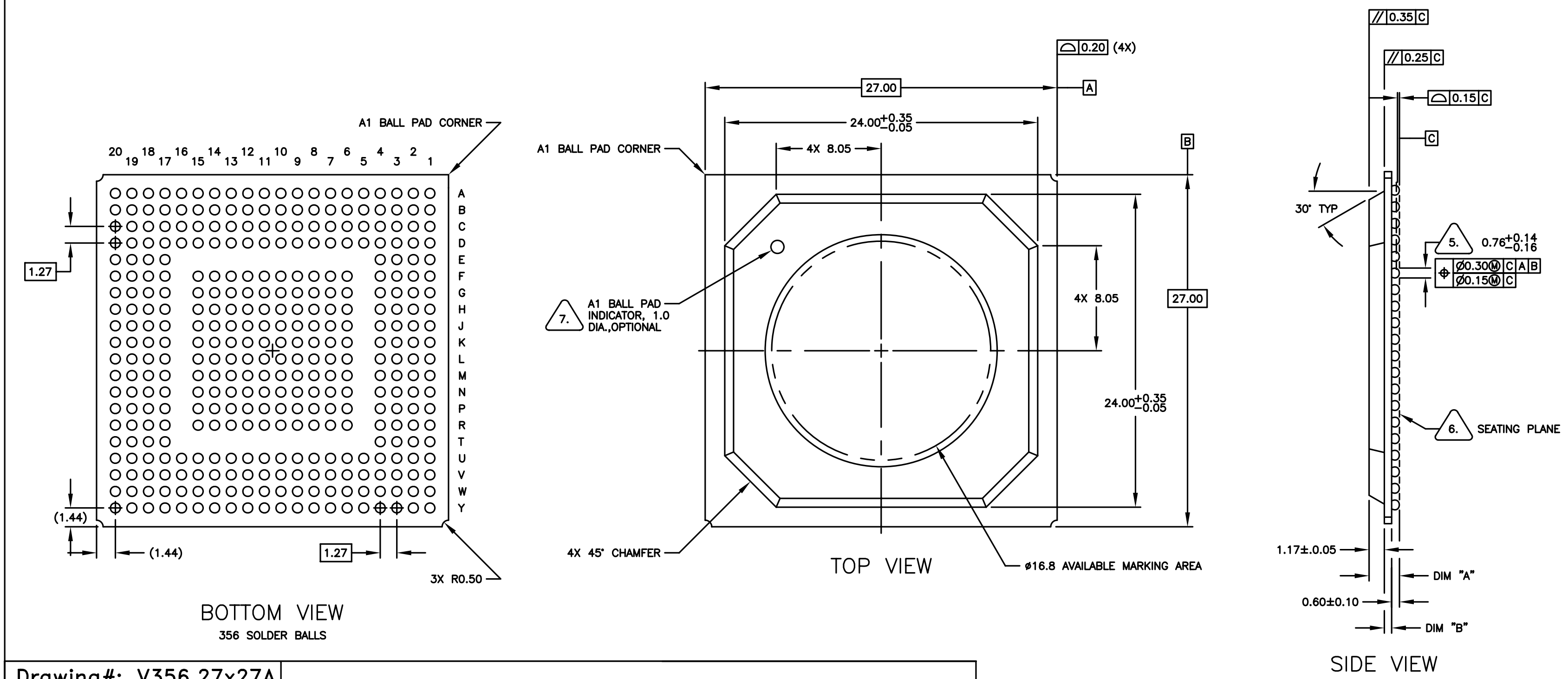
TABLE 8. θ_{JA} THERMAL RESISTANCE [°C/W]

Airflow [LFM]	0	250	500	750
No Heatsink	18	14.3	13.0	12.6
Wakefield 658-25AB Heatsink	16.0	7.0	6.0	4.7

356 Lead HBGA Package

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.27mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 20 X 20.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 400.
5. (△) DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. (△) PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. (△) A1 BALL PAD CORNER I.D. FOR PLATE MOLD: TO BE MARKED BY INK. AUTO MOLD: DIMPLE TO BE FORMED BY MOLD CAP.
8. REFERENCE SPECIFICATIONS:
   A. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS−034/A VARIATION BAL−2.



Drawing#: V356.27x27A	PACKAGE OUTLINE DRAWING − 356 HPBGA 27 x 27 mm x 1.17 mm MOLD CAP 1.27 mm PITCH SUBSTRATE
Rev: 0	
Date: 2/28/06	
Units: mm	

4	2.38±0.21	0.61±0.06	STANDARD
NO. LAYERS	DIM "A"	DIM "B"	NOTES
HPBGA THICKNESS SCHEDULE			